IN THE CLAIMS

The pending claims are as follows:

1. (Previously Presented) A method comprising:

performing a first memory access procedure, in response to receiving a first memory access procedure command over a command bus from a memory controller, wherein the first memory access procedure causes a memory module to perform multiple accesses of first memory locations associated with the memory module, and the first memory access procedure is selected from a group of procedures that includes a memory initialization procedure and a memory test procedure.

2. (Original) The method of claim 1, further comprising:

sending, over the command bus, a status message, which indicates that the memory module has completed the first memory access procedure.

3. (Original) The method of claim 1, further comprising:

receiving a second memory access procedure command over the command bus; and

performing a second memory access procedure, in response to the second memory access procedure command, wherein the second memory access procedure causes the memory module to perform multiple accesses of the first memory locations associated with the memory module, and the second memory access procedure is the memory test procedure.

4. (Original) The method of claim 3, further comprising:

sending, over the command bus, a status message, which indicates that the memory module has completed the memory test procedure.

5. (Previously Presented) A method comprising:

receiving an initialization command over a command bus from a memory controller; and

performing, within a memory module, an initialization procedure, in response to the initialization command, during which the memory module initializes one or more memory storage units by generating and sending data packets with initialization data to the one or more memory storage units.

6. (Original) The method of claim 5, further comprising:

sending, over the command bus, a status message, which indicates that the memory module has completed the initialization procedure.

7. (Original) The method of claim 5, further comprising:

performing a testing procedure, during which the memory module tests the one or more memory storage units by reading data within memory locations of the one or more memory storage units, and comparing the data with the initialization data.

8. (Previously Presented) A method comprising:

in a memory module, receiving a test command over a command bus; and

performing a testing procedure, in response to the test command, during which the memory module tests one or more memory storage units by reading data within memory locations of the one or more memory storage units, and comparing the data with expected data.

9. (Original) The method of claim 8, further comprising:

sending, over the command bus, a status message, which indicates that the memory module has completed the testing procedure.

10. (Original) The method of claim 8, further comprising:

sending, over the command bus, error information, which indicates that the memory module has encountered at least one error during the testing procedure.

11. (Original) The method of claim 8, further comprising:

performing an initialization procedure, before performing the testing procedure, during which the memory module initializes the one or more memory storage units by writing initialization data to the memory locations of the one or more memory storage units.

12. (Previously Presented) A method comprising:

a first memory module performing a first memory access procedure, in response to receiving a first memory access procedure command over a command bus from a memory controller, the first memory access procedure causing the first memory module to perform multiple accesses of first memory locations associated with the memory module, wherein the first memory access procedure is selected from a group of procedures that includes a memory initialization procedure and a memory test procedure; and

at least one additional memory module performing a second memory access procedure, in response to receiving a second memory access procedure command over the command bus from the memory controller, the second memory access procedure causing the at least one additional memory module to perform multiple accesses of second memory locations associated with the at least one additional memory module, wherein the first memory access procedure and the second memory access procedure include substantially similar process steps, and wherein at least a portion of the first memory access procedure is performed in parallel with at least a portion of the second memory access procedure.

13. (Original) The method of claim 12, wherein the first memory access procedure and the second memory access procedure include memory initialization procedures performed during an initialization of a computer system.

14. (Original) The method of claim 12, further comprising:

the first memory module performing a third memory access procedure, which causes the first memory module to perform multiple additional accesses of the first memory locations associated with the memory module, wherein the third memory access procedure is a memory test procedure; and

the at least one additional memory module performing a fourth memory access procedure, which causes the at least one additional memory module to perform multiple additional accesses of the second memory locations associated with the at least one additional memory module, wherein the fourth memory access procedure is the memory test procedure, and wherein at least a portion of the fourth memory access procedure is performed in parallel with the third memory access procedure.

15. (Original) The method of claim 14, wherein the third memory access procedure and the fourth memory access procedure include memory test procedures performed during an initialization of a computer system.

16. (Previously Presented) A method comprising:

a first memory module performing a first initialization procedure of first memory locations associated with the first memory module, wherein the first initialization procedure is performed in response to a first initialization procedure command initiating with a first processor and communicated via a first memory controller;

at least one additional memory module performing at least one additional initialization procedure of second memory locations associated with the at least one additional memory module, wherein the at least one additional initialization procedure is performed in response to at least one additional initialization procedure command originating with at least one additional processor; and

wherein at least a portion of the first initialization procedure is performed in parallel with at least a portion of the at least one additional initialization procedure.

17. (Original) The method of claim 16, further comprising:

the first memory module receiving a module initialization command; and

the first memory module initiating the first initialization procedure in response to receiving the command.

18. (Original) The method of claim 17, further comprising:

a processor generating and sending the module initialization command.

19. (Original) The method of claim 16, wherein performing the first initialization procedure comprises:

the first memory module generating and sending data packets to the first memory locations, wherein the data packets include initialization data.

20. (Original) The method of claim 16, further comprising:

the first memory module performing a first test procedure of the first memory locations; and

the at least one additional memory module performing at least one additional test procedure of the second memory locations, wherein at least a portion of the first test procedure is performed in parallel with at least a portion of the at least one additional test procedure.

21. (Previously Presented) A method comprising:

generating and sending multiple memory initialization commands to multiple memory modules of a memory subsystem, wherein the memory initialization commands are received by individual memory modules from one of one or more memory controllers;

the multiple memory modules receiving the multiple memory initialization commands; and

selected ones of the multiple memory modules performing an initialization procedure in parallel, in response to receiving an initialization command.

22. (Original) The method of claim 21, wherein performing the initialization procedure comprises:

the selected ones of the multiple memory modules generating and sending data packets to memory locations located logically behind the multiple memory modules, wherein the data packets include initialization data.

23. (Original) The method of claim 21, further comprising:

polling the selected ones of the multiple memory modules to determine when the selected ones of the memory modules have completed the initialization procedure.

24. (Original) The method of claim 21, further comprising:

a processor generating and sending multiple memory test commands to the multiple memory modules;

the multiple memory modules receiving the multiple memory test commands; and

selected ones of the multiple memory modules performing a test procedure in parallel, in response to receiving a test command.

25. (Original) The method of claim 24, further comprising:

polling each of the multiple memory modules to determine when each of the memory modules has completed the test procedure.

Claims 26. - 50. (Canceled)